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A Generalized Multilevel Inverter Topology with Reduction of Total Standing Voltage

M. JAGABAR SATHIK[1,2], (Senior Member, IEEE), DHAFER ALMAKHLES[1], (Senior Member, IEEE), S. AHAMED IBRAHIM[3], SAEED ALYAMI[4], (Member, IEEE), S. SIVAKUMAR[1], MAHAJAN SAGER BASKER[1], (Senior Member, IEEE)

[1]Renewable Energy Lab (REL), Department of Communication and networks, College of Engineering, Prince Sultan University (PSU), Riyadh 11586, Saudi Arabia. (e-mail: dalmakhles@psu.edu.sa)
[2]Department of Electrical and Electronics Engineering, SRM Institute of science and technology, Chennai, Tamil Nadu 603203, India.
[3]PRIST Deemed to be University, Thanjavur, India
[4]Electrical Engineering Department, Engineering College, Al Majma'ah University, Al Majma'ah 15341, Saudi Arabia.

Corresponding author: M. Jagabar Sathik (e-mail: mjsathik@ieee.org) and Dhafer Almakhles (e-mail: dalmakhles@psu.edu.sa)

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ABSTRACT This paper presents a new multilevel inverter topology with reduced active switches and total standing voltage. The proposed topology can generate a high number of voltage levels in the symmetric configuration. This topology intuitively generates positive and negative cycles without an additional H-bridge unit, which considerably reduces the total standing voltage of the inverter. A cascaded structure is developed from the proposed topology to create higher voltage levels. To show the novelty of the proposed topology, a thorough comparison between the available and the proposed topologies in terms of the number of switches, standing voltages, and dc-sources is presented. Furthermore, the power loss analysis is carried out for various load values. The feasibility of the proposed nine-level inverter is verified with simulation and experimental results.

INDEX TERMS Multilevel inverter, inverter, blocking voltage, cascaded structure, reduced power components.

I. INTRODUCTION

Multilevel inverters (MLIs) have gained a significant role in various applications and systems including renewable energies, active filters, flexible ac transmission system (FACTS), high-voltage dc-system (HVDC), motor drive system and electric vehicles [1]. General speaking, the MLIs are classified into three primarily topologies, namely, neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). Among these topologies, CHB is the most attractive solution due to its simple structure, modularity and easy to control. The other two MLIs, i.e., NPC and FC, require excess clamping diodes and floating capacitors to attain a high number of voltage levels [2], [3]. In CHB, the output voltage levels are generated based on the number of the cascaded units as well as the magnitude of dc-voltage sources in each unit.

The structural configurations MLI can be either symmetrical configuration where the dc-sources have value, or asymmetric configuration. In [4], a symmetric topology which consists of seven switches and a single diode is proposed for generating seven output voltage levels. However, the total standing voltage is high due to utilization of H-bridge. Another $7L$ topology is proposed in [5] which requires more bidirectional switches and components in the circuit. In [6], a $9L$ sub-MLI, which consists of four isolated dc-sources and ten switches is proposed. This sub-MLI is connected in cascade to increase the voltage levels generation; each cell has same number of isolated dc-sources with different values. In this case, individual sub-MLI works as a symmetric topology and whole cascaded structure works as an asymmetric topology. In [7], [8], the sub-MLI is extended with n number of dc-sources for any number of output voltage levels, but the standing voltage of the inverter switches significantly increases as the number of voltage levels increases. In [9], the basic unit consists of three dc-sources and five switches; another single dc-

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source unit is connected to generate all possible voltage levels. The basic unit presented in [10] consists of three dc-sources, four unidirectional switches and two bidirectional switches for eight positive voltage levels generation. The series connected of dc-sources are connected to generate the symmetric output voltage with reduced switch count is presented in [11]. However, the topologies developed in [9]–[11] use the H-bridge inverter as a polarity changer at the output terminal. The dc-sources are replaced with dc-link capacitors and extended for higher number of voltage levels. Several algorithms are presented to determine the magnitude of dc-sources in each unit, this unequal dc-source value results as uneven voltage stress and uneven power distribution on the switches. To reduce the standing voltage, the cascaded structure is discussed in [12], [13]. As presented in [14], the topology generates $9L$ voltage output with two asymmetric dc-sources using the additive and subtractive methods. The trinary geometric progression of dc-source value is proposed [14]. However, this topology needs multiple voltage rating of switches and higher voltage stress on the H-bridge inverter switches. In [15], authors proposed a new topology to generate $13L$ voltage output with four dc-sources and ten switches in each module. In [16]–[18], a novel MLI is presented with modified H-bridge and several dc-sources to increase the output voltage levels and reduce the number of high-voltage switches.

Although these topologies use reduced number of gate driver circuit, the bidirectional switches increase the switch count and size of the inverter. Another attempt is made to reduce the standing voltage of the inverter with modular based topologies which has advantage of inherent polarity changer [19], [20]. The ST-type topology uses twelve switches to generate $17L$ output voltage, the magnitude of dc-sources is selected in trinary progression method. Although, these topologies generate high number of voltage levels with a lower number of dc-sources, still the number of power switches is relatively high [19]. In [20], each module generates $9L$ and $17L$ voltage outputs with four dc-sources and ten switches in symmetric and asymmetric methods. Another topology with ten switches to generate $17L$ is proposed in [21]. In this asymmetric configuration of dc-sources are used but the maximum voltage stress on the switches is high.

This paper presents a new h-type topology which is configured in both symmetric and asymmetric method. Compared to the existing topologies, the proposed topology is developed to

- generate higher number of output voltage levels with reduced switch counts,
- have lower total standing voltage on switch,
- have a smaller number of high-voltage switch for any voltage levels generation,
- have a smaller number of ON state switches which reduces the power loss of the inverter, and
- have a smaller number of dc-source.

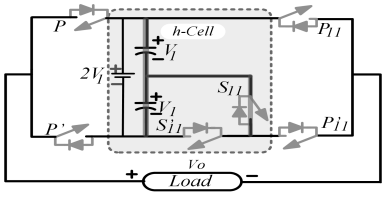

Figure 1. Proposed h-type topology generating $5L$.

This paper is organized as follows: Section II introduces the proposed topology and discussed the construction. Section III presents the extended structure of proposed h-topology and discusses the various mode of operation for $9L$ generation with mathematical expression. To generate the higher number of voltage levels, the cascaded structure of proposed h-type topology is presented in Section IV with various mathematical expression to determine the magnitude of dc-source, total standing voltage (TSV) etc., To show the effectiveness of the proposed topology in the reduction of the components and voltage stress on switches, section V compares it with other recent topologies. In section VI , the generalized power loss analysis equations are given and in section VII the simulation and experimental results with different dynamic responses are given with power loss comparison for different load power. Finally, the conclusion of proposed h-type topology with important findings of this article is given in Section VIII.

II. PROPOSED BASIC UNIT OF H-TOPOLOGY

The proposed h-type topology consists of two dc-sources or capacitors i.e., (V_1, V_1) and two switches (S_{11}, S'_{11}) as shown in Fig. 1. The switch S_{11} is connected in the midpoint of the two dc-sources and devises with output voltage V_1 and $2V_1$. The topology shown in Fig. 1 can synthesis $5L$ output voltage, namely, 0, $\pm V_{dc}$ and $\pm 2V_{dc}$ according to the switching sequence given in Table 1 where '$1'$ represents turn on and '$0'$ represents the turn off the switches. Note that the switching combinations (P, P'), (S_{11}, S'_{11}) and (P_{11}, P'_{11}) should turn on in complementary manner to avoid failing short circuit between the dc-sources and switches in all instants. It is worth stressing that the proposed topology can generate all possible odd and even voltage levels without adding a full bridge inverter in the output circuit. Furthermore, the switches (S_{11}, S'_{11}) involve in the h-cell and the switch P'_{11} withstand half of the input voltage $2V_{dc}$ and other switches (P, P', P_{11}) withstand equal value of the input voltage $2V_{dc}$. As a result, the TSV has become $\Sigma_{sv} = 10V_{dc}$. The generalized structure of proposed h-type topology with six switches and two dc-sources with equal magnitude (V_{dc}) is shown Fig. 2.

In the following section, the extended topology of the proposed h-type topology is developed to mainly generate more levels with reduced number of switches and TSV.

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Table 1. Different switching sequence for proposed h-type topology

State	P	P'	S_{11}	S'_{11}	P_{11}	P'_{11}	V_o
1	1	0	0	0	1	0	0
	0	1	0	1	0	1	
2	1	0	1	0	0	1	$+V_{dc}$
3	1	0	0	1	0	1	$+2V_{dc}$
4	0	1	1	0	0	1	$-V_{dc}$
5	0	1	0	0	1	0	$-2V_{dc}$

III. EXTENDED UNIT OF H-TYPE TOPOLOGY

In order to further increase the output voltage levels, an extended unit of h-type topology shown in Fig. 2 with n number of series connected h-cell where n is an integer number can be designed to obtain $4n+1$ number of levels. The extended structure allows producing any possible values of minimum step voltage by using a small number of h-cells. Using the same value for all the dc-sources such that $V_{1i} = V_{dc}\ \forall i = 1, \cdots, n$, implies that

$$V_{o,max} = 2nV_{dc} \tag{1}$$

where $V_{o,max}$ denotes the maximum output voltage. For example, a $9L$ voltage generation, represented in Fig. 3, consists of two series connected h-cells ($n = 2$) which implies that $V_{o,max} = 4V_{dc}$. According to this, mode of operation is explained for $9L$ inverter with corresponding current flowing paths. Table II displays the different switching combination for any number of levels (N_L) generated by an extended h-type topology with n series connected h-cells.

It is observed that the number of switches (N_{SW}) and the number of the gate driver circuit (N_{GD}) for the proposed extended unit of h-type topology with n series connected h-cells are given as $N_{SW} = N_G = 4n + 2$, respectively. According to the isolated dc-sources present in each cell, the voltage levels are generated by the proposed topology can be calculated as $N_{source} = 2n$. Based on the conducting switches and the voltage drop of the individual switches, the number of on state switches is estimated as $N_{OS} = 2n + 1$. Maximum standing voltage of each switch decides the rating of the corresponding of switch and the total standing voltage of the extended topology is obtained with addition of maximum standing voltage of the individual switches. The standing voltages of the following switches $P_1, P'_1, P_{1i}, P'_{1i}, S_{1i}, S'_{1i}$ are, respectively, represented by $V_{p_1} V_{p'_1}, V_{p_{1i}} V_{p'_{1i}} V_{s_{1i}}, V_{s'_{1i}}$ for $i = 1, \cdots n$. This implies that

$$\Sigma_{sv} = V_{p_1} + V_{p'_1} + \sum_{i=1}^{n} \left(V_{p_{1i}} + V_{p'_{1i}} + V_{s_{1i}} + V_{s'_{1i}} \right) \tag{2}$$

where Σ_{sv} denotes TVS. The switches P, P' withstand the maximum voltage as $2V_{dc}$ for any generated level and the switch $P_{1(n-1)}$ is alone withstand the highest standing voltage of the inverter as $4V_{dc}$. It is worth mentioning that the alternate switch series withstand equal voltage and the lower switches withstand lesser voltage than the upper switches. For example, the switch P_{21} withstand $2V_{dc}$ but the switch P'_{21} withstand V_{dc} and other switch voltages are measured as

$$\begin{aligned} V_{S1n} = V_{S'1n'} = V_{P'12n} &= V_{dc} \\ V_P = V_{P'} = V_{p12n} &= 2V_{dc} \\ V_{P''1(2n-1)} = 3V_{dc}, V_{P1(2n-1)} &= 4V_{dc} \\ T_{VS} = (7n+4)\, V_{dc} &= (N_L + 3\,(n+1))\, V_{dc} \end{aligned}$$

The following section presents the proposed cascaded structure of h-type inverter.

IV. PROPOSED CASCADED STRUCTURE OF H-TYPE INVERTER

The requirement of obtaining high number of levels requires more series connected h-cell in the proposed extended unit of h-type topology. As a result, greater number of symmetric dc-sources and power semiconductor devices are needed in which the TSV increases proportionally. To avoid this, a new cascaded structure shown in Fig. 4 is developed with cascaded k number of extended unit of h-type inverter where unit j uses n_j number of h-cell with $2n_j$ number of dc-capacitors for $j = 1, \cdots, k$. It implies that $N_{DC} = 2\sum_{j=1}^{k} n_j$.

The maximum output voltage of the cascaded structure is deduced as

$$V_{o,max} = \sum_{j=1}^{k} V_{oj,max} \tag{3}$$

where $V_{oj,max}$ denotes the maximum output voltage for unit j. If each unit has the same number h-cell, i.e., $n_j = n$, then

$$\begin{aligned} N_{DC} = N_{Cap} &= 2kn \\ N_{SW} = N_{GD} &= k\,(4n+2) \\ N_{Sourse} &= kn \\ N_{OS} &= k\,(2n+1)\,. \end{aligned}$$

A. DETERMINATION OF MAGNITUDE OF DC-SOURCES

It is of importance to note that the increasing number of output voltage levels is a great feature of the proposed topology. The number of dc-sources (N_{DC}) and their magnitude play crucial role in this feature. Therefore, the magnitude of each dc-source has toe be calculated which may increase the number voltage levels and reduce the number power components and dc-sources. In order to generate desired voltage levels, two design methods can be considered.

Method 1 (Uniform dc-sources): The dc-source values of the n series h-cell for all k cascaded units are uniform (have the same value) such that $V_{ji} = V_{dc}$ in in Fig. 4 for all $j = 1, \cdots, k$ for all $i = 1, \cdots, n$. In this case, each unit generate the same voltage magnitude, hence proposed works in symmetric configuration and the output voltage levels is determined as follows. Using (1) and (3), the maximum output of the circuit is obtained from $V_{o,max} = kV_{oj,max} = 2nkV_{dc}$. Then, the proposed works in

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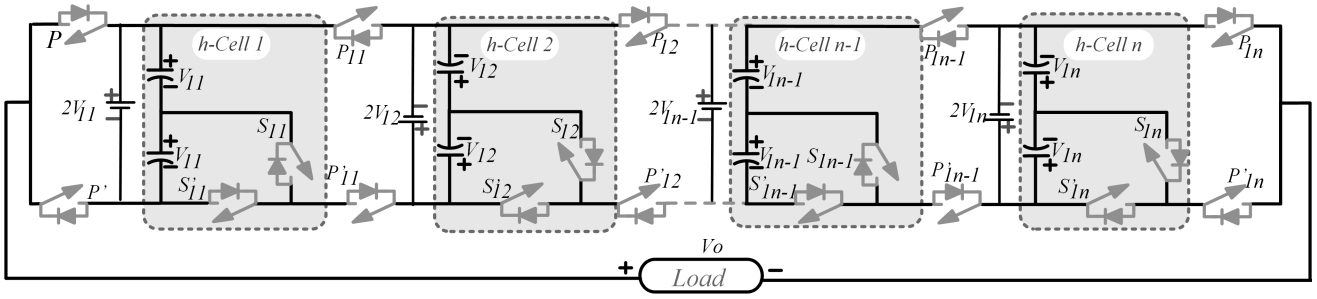

Figure 2. Generalized structure of extended h-type topology.

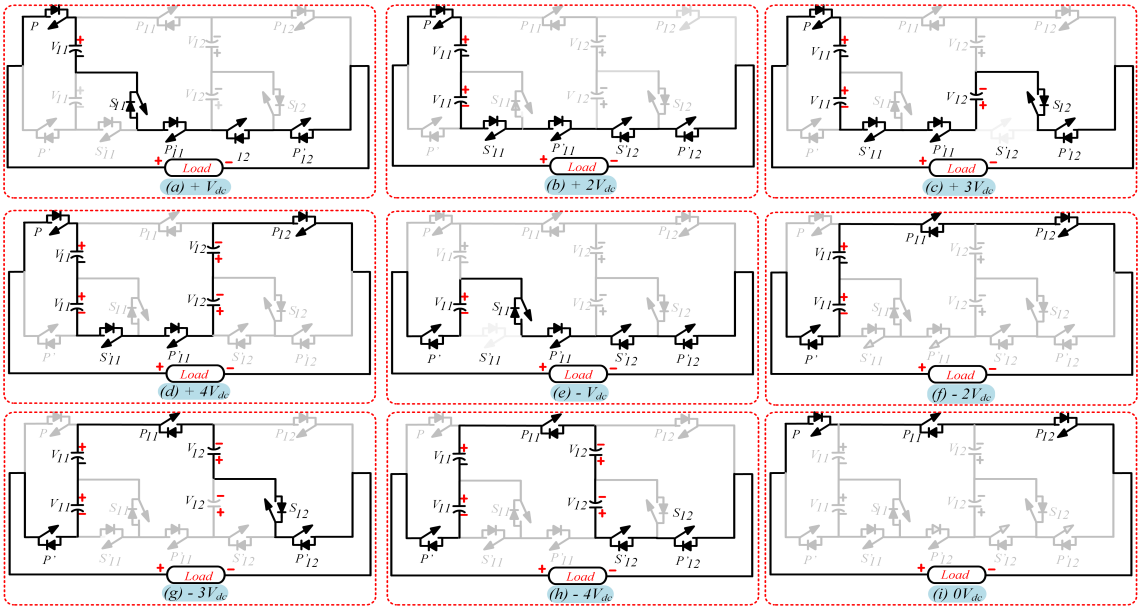

Figure 3. Various mode operations for the proposed $9L$ inverter

TABLE 2
DIFFERENT SWITCHING STATE OF EXTENDED *H*-TYPE TOPOLOGY

	Levels	P	P'	S_{11}	S'_{11}	S_{12}	S'_{12}	...	S_{1n}	S'_{1n}	P_{11}	P'_{11}	P_{12}	P'_{12}	...	P_{1n}	P'_{1n}	$V_{o,Max}$
Positive Levels	0	1	0	0	0	0	0	...	0	0	1	0	1	0	...	1	0	0
		0	1	0	1	0	1	...	0	1	0	1	0	1	...	0	1	0
	1	1	0	1	0	0	1	...	0	1	0	1	0	1	...	0	1	V_{dc}
	2	1	0	0	1	0	1	...	0	0	0	1	0	1	...	0	1	2 V_{dc}
	3	1	0	1	0	1	0	...	0	0	0	1	0	1	...	0	1	3 V_{dc}
	4	1	0	0	1	0	1	...	0	1	0	1	0	1	...	0	1	4 V_{dc}
	5	1	0	0	1	0	0	...	0	0	0	1	1	0	...	0	1	5 V_{dc}
	:	:	:	:	:	:	:	...	:	:	:	:	:	:	...	:	:	:
	n	1	0	1	0	1	0	...	1	0	0	1	0	1	...	1	1	$(n\text{-}1)*V_{dc}$
	2 n	1	0	0	1	0	1	...	0	1	0	1	0	1	...	1	0	$n*V_{dc}$
Negative Levels	-1	0	1	0	1	1	0	...	1	0	1	0	1	0	...	1	0	-1 V_{dc}
	-2	0	1	1	0	1	0	...	0	0	1	0	1	0	...	1	0	-2 V_{dc}
	-3	0	1	0	1	0	1	...	0	0	1	0	1	0	...	1	0	-3 V_{dc}
	-4	0	1	1	0	1	0	...	1	0	1	0	1	0	...	1	0	-4 V_{dc}
	-5	0	1	1	0	0	0	...	0	0	1	0	0	1	...	1	0	-5 V_{dc}
	:	:	1	:	:	:	:	...	:	:	:	:	:	:	...	:	0	:
	-(2n-1)	0	1	0	1	0	1	...	0	1	1	0	1	0	...	1	0	$-(n\text{-}1)*V_{dc}$
	-2n	0	1	1	0	1	0	...	1	0	1	0	1	0	...	1	0	$-n*V_{dc}$

symmetric configuration and generate higher voltage levels for k cascaded units as $N_L = 4nk + 1$.

Method 2 (Non-uniform dc-sources): The dc-source values of the n series h-cell for each individual units are uniform (have the same value) such that $V_{ji} = V_{dc}$ for unit j and for all $i = 1, \cdots, n$. However, it is not necessarily that all k cascaded units have the same dc-source values. In other words, the cascaded topology operates in asymmetric configuration and the output voltage and output levels are determined separately for each unit as follows:

Unit 1: All the isolated dc-sources are set as equal magnitude $V_{1i} = V_{dc}$ where $i = 1, \cdots, n$. The maximum output voltage is obtained as $V_{o1,max} = 2nV_{dc}$. The output voltage levels are obtained in first unit as $N_{L1} = 4n + 1$.

Unit k: The output voltage of the second unit is based on the voltage levels generated in the first unit; it means that a V_{dc} voltage is added into the output voltage of the first unit and fed to the second unit which is followed in all the other units. It follows that the maximum voltage and voltage

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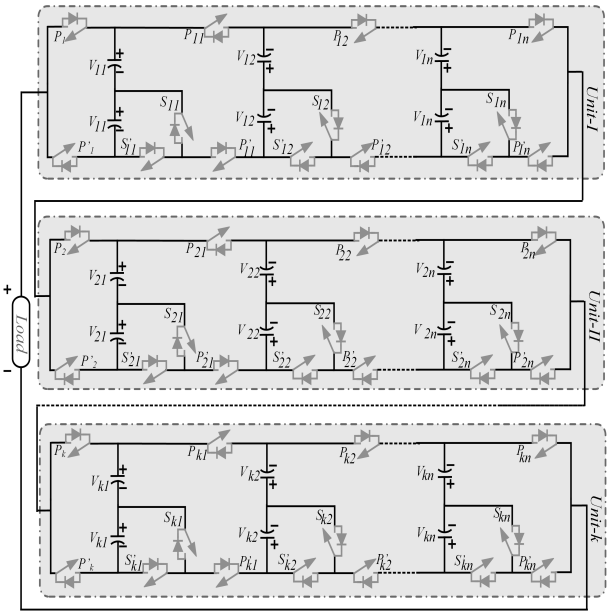

Figure 4. Cascaded Structure of proposed h-type topology.

levels of the k^{th} is deduced as follows

$$V_{ki} = 2\sum_{j=1}^{k-1} V_{j,max} + V_{dc} = (4n+1)^{k-1}V_{dc}$$

$$V_{ok,max} = 2n(4n+1)^{k-1}V_{dc}$$

and $N_{Lk} = 4n(4n+1)^{k-1}+1$ for all $i = 1, \cdots, n$, which implies

$$V_{o,max} = \left[\frac{(4n+1)^k - 1]}{n}\right] V_{dc}$$

This method can generate maximum voltage levels form the proposed cascaded topology.

B. CALCULATION OF TOTAL STANDING VOLTAGE OF H-TYPE CASCADED TOPOLOGY

The total standing voltage of the cascaded topology Σ_{sv} is sum of standing voltage of each extended topologies, which is based on the magnitude of voltage sources, and the corresponding switches connected to the sources. Consider Fig. 4, the total standing voltage of the switches

$$\Sigma_{sv} = \sum_{j=1}^{k}\left[T_{p_j} + T_{p'_j} + \sum_{i=1}^{n}\left(T_{p_{ji}} + T_{p'_{ji}} + T_{s_{ji}} + T_{s'_{ji}}\right)\right]$$

where T_{p_j},$T_{p'_j}$, $T_{p_{ji}}$, $T_{p'_{ji}}$, $T_{s_{ji}}$, and $T_{s'_{ji}}$ represent the standing voltage for switches V_{p_j},$V_{p'_j}$, $V_{p_{ji}}$, $V_{p'_{ji}}$, $V_{s_{ji}}$, and $V_{s'_{ji}}$, respectively. In general, for j cascaded unit, the standing voltage of each switch can be evaluated as

$$T_{p_j} = T_{p'_j} = 2jV_{dc},$$

$$T_{Skn} = T^{hCas}_{S'kn} = T^{hCas}_{P22n} = \frac{1}{2}T^{hCas}_{P'12n} = \frac{1}{3}T^{hCas}_{P''k(2n-1)} = \frac{1}{4}T^{hCas}_{P'k(2n-1)} = (4n+1)^k V_{dc}$$

.

The total standing voltage for k cascaded units is deduced from summation of individual units standing voltage as given equation.

V. COMPARISON OF PROPOSED CASCADED H-TYPE TOPOLOGY AND OTHER TOPOLOGIES

The proposed topology is compared with various recent topologies including symmetric [4]–[9], cascaded H-bridge inverter , cascaded module type [15]–[18], t-type [19], [20] and packed U cell [21]. Several important parameters are considered for this comparison such as number of voltage levels, switches, sources and total standing voltage. The comparison result of extended topology is listed in the Table III and the cascaded topology is shown in graphical representation. The calculated parameters are referred with number of basic units in the presented topology in Table III.

TABLE III
COMPARISON RESULTS OF PROPOSED EXTENDED TOPOLOGY AND OTHER RECENT TOPOLOGIES

Topologies	N_{Level}	N_{Switch}	N_{Gate}	N_{DC}	Diode	N_{Harv}	MBVp.u	TBV
Proposed	4n+1	4n+2	4n+2	4n		n	$(N_{Level}-1)/2$	7n+4
[7]	3n+4	n+6	2n+6	2n+1	n	4n	$(N_{Level}-1)/2$	10n+4
[8]	6n+1	10n	12n	$(N_{Level}-1)/2$	-	2n	$(N_{Level}-1)/2$	$7/3(N_{Level}-1)$
[9]	2n+1	$(N_{Level}+9)/2$	$(N_{Level}+9)/2$	$(N_{Level}-$	$(N_{Level}-1)/2$	n+3	$(N_{Level}-1)/2$	$7/3(N_{Level}-1)$
[10]	2n+1	$3/2(N_{Level}-1)$	$3/2(N_{Level}-1)$		4n	4n	$(N_{Level}-1)/2$	$5/2(N_{Level}-1)$
[11]	2n+1	$1/2(N_{Level}$	$1/2(N_{Level}$		-	2n	$(N_{Level}-1)/2$	$2(N_{Level}-1)V_{dc}$
[12]	6n+3	$5/2(N_{Level}-1)$	$5/3(N_{Level}-1)$		-	4n	$(N_{Level}-1)/2$	$3(N_{Level}-1)$
[13]	6n+1	$5/2(N_{Level}-1)$	$5/3(N_{Level}-1)$	$(N_{Level}-1)/2$	-	4n	$(N_{Level}-1)/2$	$(3\ N_{Level}-2)$
[15]	8n+3	$(N_{Level}-1)$	$(N_{Level}-1)$		-	4n	$(N_{Level}-1)/2$	$3(N_{Level}-1)$
[16]	4n+3	$3(N_{Level}-1)/2$	$4(N_{Level}-1)/3$		n	4n	$(N_{Level}-1)/2$	$(3\ N_{Level}-2)$
[17]	2n+1	5n+1	4n+1		-	4n	$(N_{Level}-1)/2$	$(4\ N_{Level}-1)$

Fig. 5.(a) shows the comparison of voltage levels and required number of switches, the conventional CHB and presented topology in [16] need higher number of switches for same number of voltage levels. The recent topologies presented in [17], [18], [20], [21] use same number of switches for any voltage levels generation. The topologies presented in [7], [18] use equal number switch and gate driver circuit since all switches are unidirectional switches, other topologies use bidirectional switches which increase the number of IGBTs. It is important to note, the topologies presented in [8] and [18] required additional diodes in each unit which make voltage spikes in the output waveform but it is not in the proposed topology. However, the proposed h-topology generates a higher number of voltage levels with

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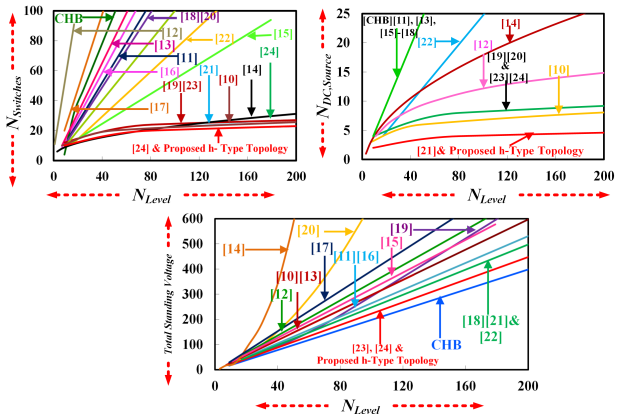

Figure 5. (a) Comparison of voltage level and switches (b) Comparison of voltage level and dc-sources (c) Comparison of voltage level and total standing voltage.

fewer switch count than other topologies. In Fig. 5.(b), the presented topologies in [14], [15], [17], [21] require equal number of dc-sources. Even though, the proposed topologies in [18], [19] use asymmetric values, the required number of dc-sources are high for desired voltage levels generation than the proposed topology. It is worth mentioning that the presented topology in [21] use two dc-sources and boost capacitors for same voltage levels generation of proposed topology which required additional circuit for capacitor voltage balancing for each voltage levels generation.

The voltage rating of the switch and cost of the inverter depends on the voltage stress of switches. The presented topologies in [7], [10], [13] need additional H bridge circuit for polarity changing in each unit which result the increase of total standing voltage and required high-voltage switches of the inverter as shown in Fig. 5.(c). In [10], [16]–[18], [20], [21] are packed U-cell type topologies which need two high-voltage switches in each unit. However, the proposed topology has a single high-voltage switches in each unit but other topologies require minimum two switches which is remarkable advantage of the proposed topology. In order to clarify the cost value, the Table IV compares the proposed and other cascaded topologies [5]–[21]. The cost function is based on the number of power components and standing voltage on the switches. In addition, cost factor ($\alpha = 0.5$ or $\alpha = 1$) and standing voltage are major role, which are multiplied with the standing voltage (TBVp.u.) and total number of components accordingly. In Table V, $9L$ nine level inverters are considered but the cascaded topologies presented in [10], [11] does not generate exact $9L$, therefore closes to $9L$ output is considered and compared.

TABLE 4
COMPARISON RESULTS OF PROPOSED CASCADED TOPOLOGY AND OTHER RECENT TOPOLOGIES

Topologies	N_{Level}	N_{Switch}	N_{Gate}	N_{DC}	N_{Diode}	$N_{Rswitch}$	MSV	TSV
Proposed	9^*	$10k$	$10k$	$2k$	-	k	$4V_{dc}$	$9/4(N_{Level}-1)\ V_{dc}$
CHB	3^*	$4k$	$4k$	k	-	-	V_{dc}	$2(N_{Level}-1)\ V_{dc}$
[9]	$6k+1$	$8k$	$8k$	$3k$	2 k	$4k$	$4V_{dc}$	$5/2(N_{Level}-1)V_{dc}$
[10]	7^*	$10k$	$10k$	$3k$	-	$3k$	$3V_{dc}$	$3(N_{Level}-1)V_{dc}$
[13]	13^*	$12k$	$10k$	$3k$	-	$4k$	$6V_{dc}$	$3(N_{Level}-1)V_{dc}$
[14]	7^*	$8k$	$7k$	$2k$	-	$4k$	$4V_{dc}$	$3(N_{Level}-1)V_{dc}$
[16]	7^*	$9k$	$8k$	$3k$	k	$4k$	$3V_{dc}$	$8/3(N_{Level}-1)V_{dc}$
[18]	$6n+1$	$10k$	$8k$	$4k$	-	$4n$	$4V_{dc}$	$3(N_{Level}-1)\ V_{dc}$
[19]	9^*	$12k$	$10k$	$4k$	-	$2k$	$4V_{dc}$	$3(N_{Level}-1)V_{dc}$
[20]	9^*	$10k$	$8k$	$4k$	-	$2k$	$4V_{dc}$	$5/2(N_{Level}-1)V_{dc}$
[21]	9^*	$10k$	$10k$	$2k$	2 k	$2k$	$4V_{dc}$	$11/4(N_{Level}-1)V_{dc}$
[22]	$16n+1$	$12k$	$9k$	k	-	$2k$	$4V_{dc}$	$5/2(N_{Level}-1)\ V_{dc}$
[23]	9^*	$12k$	$10k$	$4k$	-	$2k$	$4V_{dc}$	$9/4(N_{Level}-1))V_{dc}$
[24]	9^*	$10k$	$10k$	$4k$	-	$2k$	$4V_{dc}$	$9/4(N_{Level}-1)V_{dc}$

TABLE 5
COST BASED COMPARISON OF PROPOSED AND RECENT MULTILEVEL INVERTER TOPOLOGIES

Topologies	N_{Level}	N_{Switch}	N_{Gate}	N_{DC}	N_{Diode}	$N_{Capacitor}$	MSV	TSV	$TSV_{P.U}$	SUF	Cost	
											$\alpha=0.5$	$\alpha=1$
Proposed	9	10	10	2	0	4	$4\ V_{dc}$	$18\ V_{dc}$	4.5	1.1	5.3	5.8
CHB	9	16	16	4	0	0	V_{dc}	$16V_{dc}$	4	1.7	15.1	16
[10]	9	12	12	4	0	0	$4V_{dc}$	$20V_{dc}$	5	1.3	11.8	12.9
[11]	9	9	9	4	0	0	$4V_{dc}$	$22V_{dc}$	5.5	1	9.2	10.4
[12]	9	10	10	4	0	0	$4V_{dc}$	$24V_{dc}$	6	1.1	10.2	11. 6
[13]	7	10	10	3	0	0	$3V_{dc}$	$18V_{dc}$	6	1.4	7.6	8.6
[14]	7	8	7	3	0	0	$3V_{dc}$	$18V_{dc}$	6	1.1	6	7.1
[15]	11	10	10	5	0	0	$5V_{dc}$	$34V_{dc}$	8.5	0.9	13.4	15.83
[16]	9	9	8	4	1	0	$4V_{dc}$	$24V_{dc}$	6	1	9.3	10.6
[17]	9	10	8	4	0	0	$4V_{dc}$	$20V_{dc}$	5	1.1	9.1	10.2
[18]	9	20	17	4	0	0	$4V_{dc}$	$24V_{dc}$	6	2.2	17.8	19.1
[19]	9	12	10	4	0	0	$4V_{dc}$	$24V_{dc}$	6	1.3	11.1	12.4
[20]	9	10	8	4	0	0	$4V_{dc}$	$20V_{dc}$	5	1.1	9.1	10.2
[21]	9	10	10	2	2	2	$4V_{dc}$	$22V_{dc}$	5.5	1.1	5.9	6.5
[23]	9	12	10	4	0	0	$4V_{dc}$	$18V_{dc}$	4.5	1.3	10.8	11.8
[24]	9	10	10	4	0	0	$4V_{dc}$	$20V_{dc}$	4.5	1.1	9.9	10. 9

The topologies presented in [20], [21] have equal standing voltage with proposed topology but the cost function is high compared proposed topology due to increase of gate driver circuit and dc-sources. Considering CHB, the proposed topology has higher standing voltage but the proposed topology have cost function is low since the CHB require increased number of components and given by

$$CF = (N_{SW} + N_D + N_{GD} + N_C + \alpha TBV_{p.u})\, N_{source}$$

where CFstands for cost function.
[1]

VI. SIMULATION AND EXPERIMENTAL RESULTS

The performance of proposed h-type topology is analysed with $9L$ nine level prototype inverter as shown in Fig. 6. In order to generate output voltage levels, two h-cells are connected in series with four dc-sourcesV_1 and V_2 with equal magnitude of $30V$. These two cells can generate the possible voltage levels as 0, $\pm 30V$, $\pm 60V$, $\pm 90V$, $\pm 120V$ in the output. The simulation results are obtained through MATLAB/ Simulink software. The Nearest Level Control (NLC) is employed as modulation technique for gate pulse generation to each switch and the voltage and current waveform is captured in Fig. 7.(a). It can be observed from the Fig.7.(b) & (c), the maximum output voltage is obtained as 120 V and the corresponding THD is 9.33% respectively.

[1] $^*k$- number of cascaded unit, n-number of basic unit

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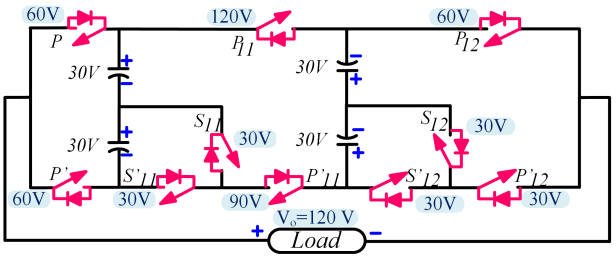

Figure 6. Experimental diagram of the proposed $9L$ inverter.

The load current is observed as $3.7A$ for the given resistive inductive (RL) value as $R = 30\Omega$ and $L = 40mH$. This R-L load considerably reduces the current harmonics as 1.33% since it act as low pass filter circuit in the output circuit as shown in Fig. 7. (b). The standing voltage on the switches $P_{11} = 120V$, $P'_{11} = 90V$, $P' = 60V$, $S_{11} = 30V$ and $S'_{12} = 30V$ are shown in Fig. 7.(c). In this, complementary switches P and P' withstand same magnitude of voltage. However, the switches in the first leg P_{11} and P'_{11} withstand the maximum voltage as $120V$, $90V$ respectively, switch P_{12} capable to withstand $60V$, and other switches create standing voltage as $30V$. It is clear evident, the switch S'_{11} alone withstands high-voltage in the inverter, which results that the proposed h-type topology is suitable for the high-voltage application.

TABLE 6
THE DETAILS OF SIMULATION AND EXPERIMENTAL PARAMETERS

Output Parameters	Simulation Results	Experimental Results
Input voltage	V_1=V_2= 30V	V_1=V_2= 30V
IGBT (IRF450)	-	500V/ 14 A
Driver circuits	-	Up to 1200V (TLP 250)
Load value	R=50 Ω, L=60mH / R=30 Ω, L=40 mH	
Maximum output voltage	120 V	
Output current	2.23 A/ 3.7 A	2.2 A/ 3.7 A
Output power	133.64 W	128.32 W
Efficiency	98.81%	95.22%

An experimental model is developed for the circuit as depicted in Fig. 6. The switch is IRF450 IGBT and driver circuits is TLP250 up to $1200V$ is used. The dead time is generated as $4s$ with RC circuit to prevent the short circuit when the switching transition of complementary switches. The $R-L$ load value is assumed as same value of simulation as $R = 30\Omega$ and $L = 40mH$ and the rest of the parameters are given in Table VI. The output voltage and current for this load value is $120V$ and $3.7A$ respectively as shown in Fig. 8.(a). The prototype model of proposed h-type inverter is shown in Fig. 10.

The dynamic performance of the proposed topology is tested with sudden variation in load values; it is shown in the Fig. 8.(b)-(f). In Fig. 8.(b), the sudden load change is captured between the resistance value is $(50 - 30)\Omega$ and inductance values is $(40 - 60)mH$. The current value is increased from $2.2A$ to $3.7A$ and then the current value reaches to zero in zero load condition in Fig.8.(c) and the current value is increased from zero to $2.2A$, but the voltage is remains constant as shown in Fig. 8.(d). This gradual current variation and the constant output voltage is based on the load changes, which indicates the dynamic performance of the proposed topology. Another analysis of the proposed topology is carried out with the different modulation index. The modulation index is ratio between the amplitude of modulation signal and carrier signal which is considered within $(0-1)$. Fig.8.(e) gives the voltage and current waveform for the modulation index is 0.4 and it show the level transition from three levels to five levels. Then, the Fig. 8.(f) shows the voltage levels variation from $5L$ five level to $9L$ nine level for modulation index 0.6 to 1.0. As can be seen from Table VI, the output power and efficiency is obtained for the proposed topology is $133.64W$ and 98.8% respectively.

To investigate the performance of the h-type MLI, power loss analysis is carried for various power ratings such as $0.5kW$, $1.0kW$, $1.5kW$, $2.5kW$ and $5.0kW$ of the load as shown Fig. 9.(a)-(e). The results of these power loss and efficiency is plotted in Fig. 9.(f). The maximum efficiency of the proposed inverter is obtained as 98.8% with reduced losses.

VII. CONCLUSIONS

The proposed topology used lower number of power electronics components and reduced dc-sources. Further, the maximum voltage stress on the switch is reduced to $4V_{dc}$ for any number of voltage levels in symmetric configuration which is more suitable for medium voltage applications. The simulated and experimental results are presented for various load values. The sudden load changes and modulation index variations are applied to the proposed topology and it corresponding results are given. Further, the power loss and efficiency of propose topology presented for various load power. It is confirming that the proposed topology is more suitable various load changing applications like AC drives, grid connected PV system etc.

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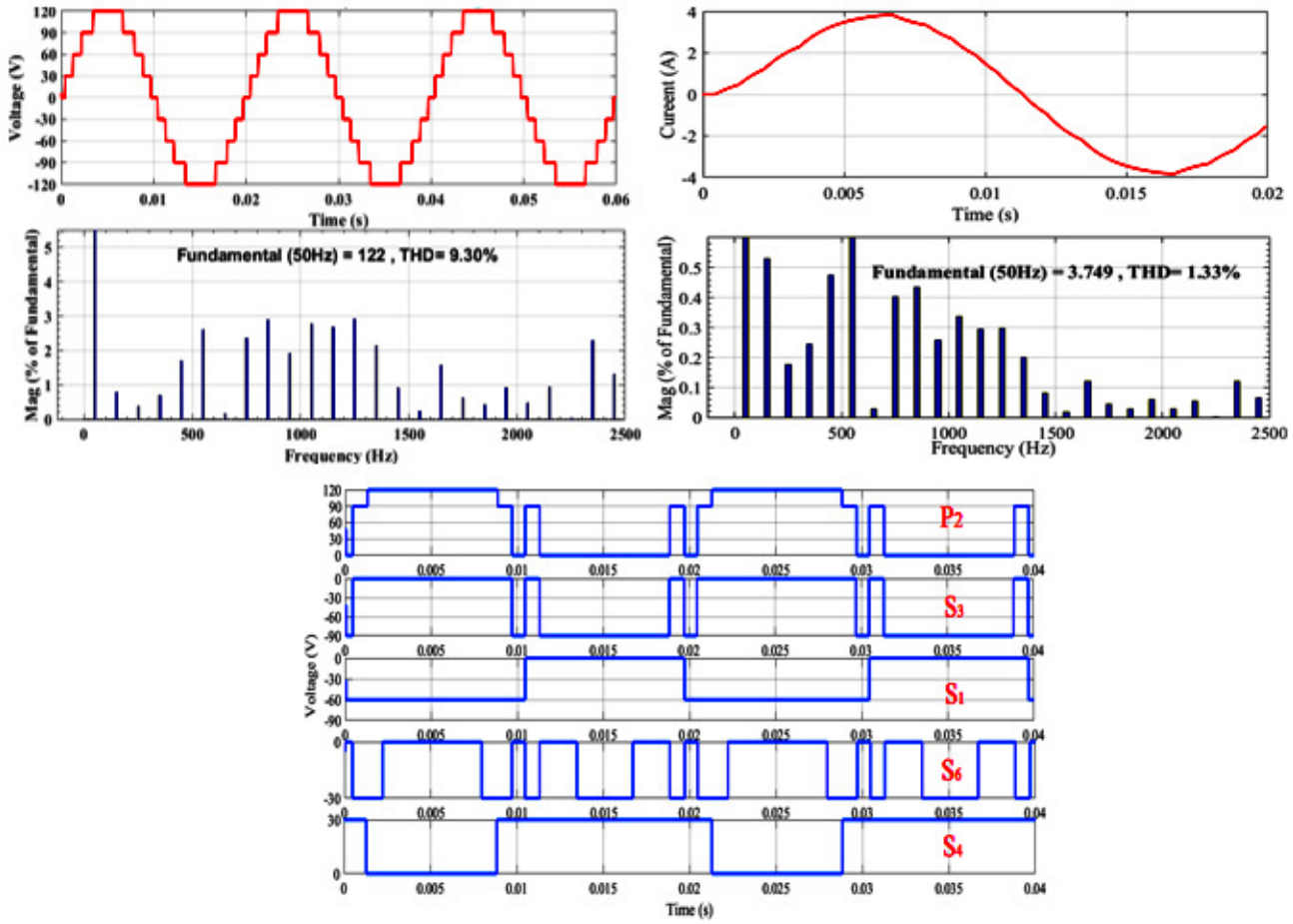

Figure 7. Simulation results of the proposed $9L$ inverter for $R = 30\ \Omega$, $L = 40mH$ a) Output voltage waveform with FFT spectrum, b) Output Current with FFT spectrum and (c) blocking voltage on switches P_2, S_3, S_1, S_6, S_4.

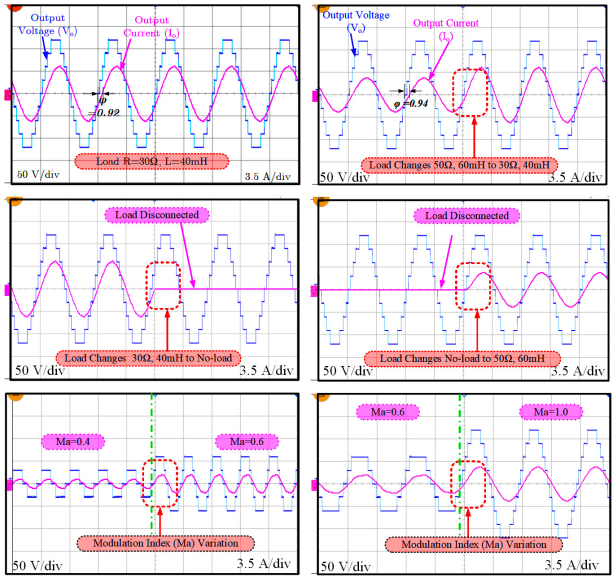

Figure 8. Experimental results of Output voltage and current waveform for proposed $9L$ inverter (a) at load 30 Ω-40mH, dynamic load changes (b) from 50 Ω-60 mH to 30 Ω-40 mH, (c) from 30 Ω-40 mH to no-load (d) from no-load to $50\Omega - 60$ mH and modulation index variations (e) from 0.4 to 0.6 and (f) from 0.6 to 1.0.

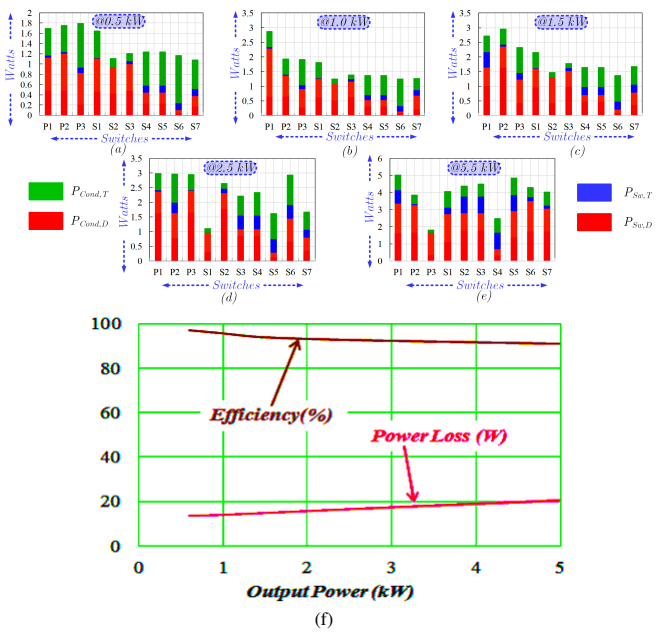

Figure 9. $P_{Cond,T}$, $P_{Cond,D}$, $P_{Sw,T}$, and $P_{Sw,D}$ (a) at 0.5kW (b) at 1.0kW, (c) at 1.5kW\ (d) at 2.5kW (e) at 5.5kW and (f) Power Efficiency and Loss

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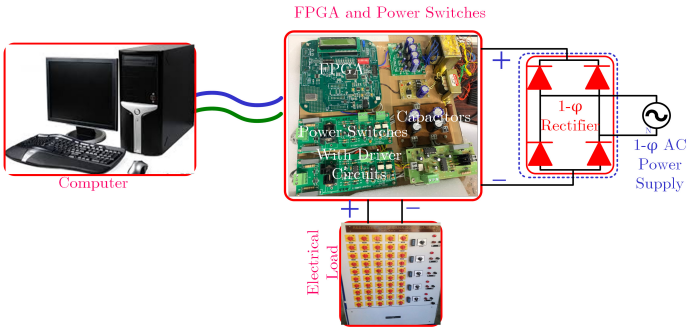

Figure 10. Experimental Setup.

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Jagabar Sathik Mohamed Ali (Senior Member, IEEE) was born in Thanjavur, India, in 1979. He received the B.E. degree in electronics and communication engineering from Madurai Kamarajar University, Madurai, India, in 2002, and the M.E. and Ph.D. degrees from the Faculty of Electrical Engineering, Anna University, Chennai, India, in 2004 and 2016, respectively. He is currently a Postdoctoral Fellow with the Renewable Energy Lab, College of Engineering Department, Prince Sultan University, Riyadh, Saudi Arabia. He is a Consultant of various power electronics companies for the design of power electronics converters in India. He has authored more than 30 articles publications in international peer-reviewed journals and conference proceedings. His research interests include multilevel inverters, grid-connected inverters, and power electronics converters and its applications to renewable energy systems. He is serving as a Regular Reviewer for several journals, including the IEEE Transactions on Industrial Electronics, Transactions on Power Electronics, IET Power Electronics, and IEEE Access.

Dhafer J. Almakhles (M'13, SM'20) received the B.E. degree in electrical engineering from the King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, in 2006, and the master degree (Hons.) and Ph.D. degree from The University of Auckland, New Zealand, in 2011 and 2016, respectively. Since 2016, he has been with Prince Sultan University, Saudi Arabia, where he is currently the Chairman of the Communications and Networks Engineering Department, and the Director of the Science and Technology Unit and Intellectual Property Office, Prince Sultan University. He is the Leader of the Renewable Energy Research Team and Laboratory. His research interests include power electronics, control theory, crewless aerial vehicles, renewable energy systems, and FPGA applications. He is a member of the IEEE Power Electronics and the IEEE Control Society. He is a Reviewer Member of various international journals and conferences, including the IEEE and IET.

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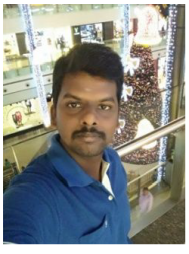
Ahamed Ibrahim S. A. was born in Kadayanallur, India, in 1985. He received the B.E. degree in Electrical and Electronics Engineering from the Anna University, Chennai, India, in 2006 and the M.E. degree in Power System Engineering from Anna University, Chennai, India, in 2011. He received the PhD degree in Electrical Engineering in Anna University, Chennai in 2019. He is currently working as an Assistant Professor in PRIST University, Thanjavur, india Since 2019. His current research interests include power electronic converters, Multilevel Converters, Renewable energy sources.

SAEED ALYAMI received the B.S. degree in electrical engineering from the King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, in 2004, and the M.S. and Ph.D. degrees in electrical and computer engineering from Wayne State University, Detroit, MI, USA, in 2010 and 2016, respectively. From 2004 to 2008, he was a Power Transmission Engineer with the Engineering and Design Department for Substations and Grid Integration, Saudi Electricity Company, Saudi Arabia. He is currently an Assistant Professor with Majmaah University. His research interests include smart grid, control of renewable energy systems, and distributed generation.



SIVAKUMAR SELVAM was born in Tamilnadu, India, in 1991. He received his B.E. degree in Electrical and Electronics Engineering, and M.E. degree specialized in Power Electronics and Drives from Anna University, Chennai in 2013 and 2015 respectively. He is currently working as Research Assistant in Renewable Energy Laboratory, Prince Sultan University, Saudi Arabia. His research interest includes Grid interfaced Solar PV systems, Multilevel Inverters, DC-DC converters for Microgrid applications, and Digital Control of Power converters

Mahajan Sagar Bhaskar (Senior Member, IEEE) received the bachelor degree in electronics and telecommunication engineering from the University of Mumbai, Mumbai, India, in 2011 and the master degree in power electronics and drives from VIT University, India, in 2014, and the Ph.D. degree in electrical and electronic engineering, University of Johannesburg, South Africa, in 2019. He worked as a Researcher Assistant with the Department of Electrical Engineering, Qatar University, Doha, Qatar, from 2018 to 2019. He worked as a Research Student with the Power Quality Research Group, Department of Electrical Power Engineering, Universiti Tenaga Nasional (UNITEN), Private University, Kajang, Kuala Lumpur, Malaysia, from August 2017 to September 2017. He is currently with the Renewable Energy Lab, Department of Communications and Networks Engineering, College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia. He has authored 100 plus scientific articles particular reference to X.Y. converter family, multilevel DC/DC and DC/AC converter, and high-gain converter. He received the Best Paper Research Paper Awards from the IEEE-CENCON 19, IEEE-ICCPCT 14, IET-CEAT 16, and ETAEERE 16 sponsored Lecture note in electrical engineering, (Springer). He is a member of the IEEE Industrial Electronics, Power Electronics, Industrial Application, and Power and Energy, Robotics and Automation, Vehicular Technology Societies, Young Professionals, various IEEE Councils and Technical Communities. He is a Reviewer Member of various international journals and conferences including IEEE and IET. He received the IEEE Access Award Reviewer of Month, in January 2019, for his valuable and thorough feedback on manuscripts, and for his quick turnaround on reviews.

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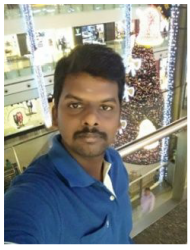
SAEED ALYAMI received the B.S. degree in electrical engineering from the King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, in 2004, and the M.S. and Ph.D. degrees in electrical and computer engineering from Wayne State University, Detroit, MI, USA, in 2010 and 2016, respectively. From 2004 to 2008, he was a Power Transmission Engineer with the Engineering and Design Department for Substations and Grid Integration, Saudi Electricity Company, Saudi Arabia. He is currently an Assistant Professor with Majmaah University. His research interests include smart grid, control of renewable energy systems, and distributed generation.



SIVAKUMAR SELVAM was born in Tamilnadu, India, in 1991. He received his B.E. degree in Electrical and Electronics Engineering, and M.E. degree specialized in Power Electronics and Drives from Anna University, Chennai in 2013 and 2015 respectively. He is currently working as Research Assistant in Renewable Energy Laboratory, Prince Sultan University, Saudi Arabia. His research interest includes Grid interfaced Solar PV systems, Multilevel Inverters, DC-DC converters for Microgrid applications, and Digital Control of Power converters

Mahajan Sagar Bhaskar (Senior Member, IEEE) received the bachelor degree in electronics and telecommunication engineering from the University of Mumbai, Mumbai, India, in 2011 and the master degree in power electronics and drives from VIT University, India, in 2014, and the Ph.D. degree in electrical and electronic engineering, University of Johannesburg, South Africa, in 2019. He worked as a Researcher Assistant with the Department of Electrical Engineering, Qatar University, Doha, Qatar, from 2018 to 2019. He worked as a Research Student with the Power Quality Research Group, Department of Electrical Power Engineering, Universiti Tenaga Nasional (UNITEN), Private University, Kajang, Kuala Lumpur, Malaysia, from August 2017 to September 2017. He is currently with the Renewable Energy Lab, Department of Communications and Networks Engineering, College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia. He has authored 100 plus scientific articles particular reference to X.Y. converter family, multilevel DC/DC and DC/AC converter, and high-gain converter. He received the Best Paper Research Paper Awards from the IEEE-CENCON 19, IEEE-ICCPCT 14, IET-CEAT 16, and ETAEERE 16 sponsored Lecture note in electrical engineering, (Springer). He is a member of the IEEE Industrial Electronics, Power Electronics, Industrial Application, and Power and Energy, Robotics and Automation, Vehicular Technology Societies, Young Professionals, various IEEE Councils and Technical Communities. He is a Reviewer Member of various international journals and conferences including IEEE and IET. He received the IEEE Access Award Reviewer of Month, in January 2019, for his valuable and thorough feedback on manuscripts, and for his quick turnaround on reviews.